Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **Q12**
2. **Q13**
3. **Q14**
4. **Q6**
5. **Q5**
6. **Q7**
7. **Q4**
8. **VSS**
9. **Q1**
10. **Ø**
11. **RESET**
12. **Q9**
13. **Q8**
14. **Q10**
15. **Q11**
16. **VDD**

**.086”**

**.099”**

**14 13 12 11**

**10**

**9**

**8**

**7**

**3 4 5 6**

**15**

**16**

**1**

**2**

**DIE ID**

**CD4020B**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VDD**

**Mask Ref: CD4020B**

**APPROVED BY: DK DIE SIZE .086” X .099” DATE: 8/25/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .011” P/N: CD4020BH**

**DG 10.1.2**

#### Rev B, 7/1